CLAIMS

1. A decoder block comprising:

a number N of generic decoder blocks, each generic block including

a plurality of decoders, and

a plurality of block address signal lines,

where the number of block address signal lines is less than or equal to $2*(2^k-1)+2(N-1)$, where k= is the whole number portion of $\log_2(N-1)$.

2. The decoder block of claim 1, wherein the decoder comprises a gray code decoder block.

3. The decoder block of claim 1, wherein the decoder block comprises a binary decoder block.

4. The decoder block of claim 3, wherein the number of block address signal lines is less than or equal to $2*(2k-1)+N$.

5. A decoder block comprising:

a plurality of generic decoder blocks arranged in series, each generic block having

an m-bit block address,

a plurality of decoders, and

a plurality of block address signal lines grouped into sections, each section corresponding to a bit-position of an m-bit block address

wherein the number of block address signal lines in the generic block is less than or equal to $2*(2^k-1)+2(N-1)$, where k is the whole number portion of $\log_2(N-1)$.

6. The decoder block of claim 5, wherein a top signal line in the section corresponding to the least significant bit of the block address changes in the sequence [01] across the series generic blocks.

7. The decoder block of claim 5, wherein the decoder block comprises a binary decoder block.

8. The decoder block of claim 7, wherein the number of block address signal lines in the generic block is less than or equal to $2*(2^k-1)+N$.

9. The decoder block of claim 7, wherein the each decoder in each decoder block includes an addressing signal line connected to a top block address signal line in each section.

10. The decoder block of claim 7, wherein a top block address signal line in the section corresponding to the

second most significant bit of the block address changes in the sequence [0011] across the series generic blocks.

11. The decoder block of claim 5, wherein the decoder block comprises a gray code decoder block.

12. The decoder block of claim 11, wherein a top block address signal line in the section corresponding to the second most significant bit of the block address changes in the sequence [0110] across the series generic blocks.

13. A decoder block comprising:

a number N of generic decoder blocks, each generic block having an m-bit block address and including

a plurality of decoders,

no more than N block address signal lines, and

an m-bit block address decoder coupled to said N block address signal lines.

14. The decoder block of claim 13, wherein the generic decoder block are stitched together in a series.

15. The decoder block of claim 12, wherein the decoder block comprises a binary decoder.

16. The decoder block of claim 12, wherein the decoder block comprises a gray code decoder.

17. The decoder block of claim 12, wherein the each generic decoder block includes a plurality of decoder address signal line pairs, wherein the lines in one of said address signal line pairs switch position between adjacent generic blocks.

18. An image sensor comprising:

a pixel section having a first pitch, and

a decoder section having a second pitch,

wherein the second pitch is smaller than the first pitch.

19. The image sensor of claim 18, wherein the decoder section comprises a plurality of generic blocks stitched together in a series, wherein adjacent generic blocks are separated by a stitching section including routing lines operative to connect signal lines in the adjacent generic blocks.

20. The image sensor of claim 18, further comprising a plurality of interconnect lines connected between the pixel section and the decoder section, wherein two or more

of said interconnect lines are connected at an angle to accommodate the stitching sections.

21. A method comprising:

patterning a pixel section including pixel features having a first pitch on a surface; and

patterning a decoder section including features having a second pitch which is smaller than the first pitch on the surface.

22. The method of claim 21, wherein a ratio of the second pitch to the first pitch is less than approximately 0.98.

23. The method of claim 22, wherein the first pitch is approximately 9 μm and the second pitch is approximately 8.75 μm.

24. The method of claim 21, wherein a ratio of the second pitch to the first pitch is less than approximately 0.95.

25. The method of claim 24, wherein the first pitch is approximately 18 μm and the second pitch is approximately 17 μm.